



WINSTAR Display Co.,Ltd.
華凌光電股份有限公司



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SPECIFICATION

MODULE NO.: WF101JSYAHMNBO#

General Specifications

| Item | Dimension | Unit |
|------------------|--|------|
| Size | 10.1 | inch |
| Dot Matrix | 1024 RGB x 600 | dots |
| Module dimension | 235(W) x143(H) x 8.78(D) | mm |
| Active area | 222.72 (H) x 125.28(V) | mm |
| Pixel pitch | 0.2175(W) x 0.2088(H) | mm |
| LCD type | TFT, Normally Black, Transmissive | |
| TFT Interface | 4-Lanes MIPI | |
| Driver IC | EK79007AD3 + EK73217BCGA or equivalent | |
| Viewing Angle | 85/85/85/85 | |
| Aspect Ratio | 16:9 | |
| Backlight Type | LED, Normally White | |
| PCAP IC | ILLI2511 or equivalent | |
| PCAP Interface | USB (I2C available) | |
| PCAP FW Version: | V6.0.0.0.62.90.1.2 | |
| Touch Panel | Projected capacitive Touch Panel | |
| Surface | Glare | |

*Color tone slight changed by temperature and driving voltage.

Absolute Maximum Ratings

| Item | Symbol | Min | Typ | Max | Unit |
|-----------------------|--------|-----|-----|-----|------|
| Operating Temperature | TOP | -20 | — | +70 | °C |
| Storage Temperature | TST | -30 | — | +80 | °C |

Electrical Characteristics

Typical Operation Conditions (At Ta = 25 °C,)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|--------------------------------------|---------------------|-------|-------|------|------|
| Digital Power Supply Voltage For LCD | VDD | 1.71 | 1.8 | 1.89 | V |
| Analog Power Supply Voltage | AVDD | 9.89 | 10.2 | 10.5 | V |
| Gate On Power Supply Voltage | VGH | 19.4 | 20.0 | 20.6 | V |
| Gate Off Power Supply Voltage | VGL | -10.3 | -10.0 | -9.7 | V |
| Common Power Supply Voltage | VCOMI | 4.0 | 4.3 | 4.6 | V |
| Supply PCAP | VDDT | 3.0 | 3.3 | 3.6 | V |
| | I _{VDDT} | | 90.5 | 115 | mA |
| | USB_VDD 5V | 4.4 | 5.0 | 5.5 | V |
| | I _{VDD 5V} | — | 97.8 | 120 | mA |

Interface

1.TFT LCD MODULE

| Pin No. | Symbol | Description |
|---------|--------|--|
| 1 | VLED+ | LED Anode |
| 2 | VLED+ | LED Anode |
| 3 | VGH | Positive power for TFT |
| 4 | VGL | Negative power for TFT |
| 5 | UPDN | Gate up or down scan control. UPDN = "L", STV2 output vertical start pulse and UD pin output logical "L" to Gate driver. (default) UPDN = "H", STV1 output vertical start pulse and UD pin output logical "H" to Gate driver |
| 6 | SHLR | Source right or left sequence control. SHLR = "L", shift left: last data = S1←S2←S3.....←S1536 = first data. SHLR = "H", shift right: first data = S1→S2→S3.....→S1536 = last data.(default) |
| 7 | VLED- | LED Cathode |
| 8 | VLED- | LED Cathode |
| 9 | AVDD | Analog power |
| 10 | GND | Digital ground |
| 11 | D3P | MIPI data input. |
| 12 | D3N | MIPI data input. |
| 13 | GND | Digital ground |
| 14 | D2P | MIPI data input. |
| 15 | D2N | MIPI data input. |
| 16 | GND | Digital ground |
| 17 | CLKP | MIPI clock input |
| 18 | CLKN | MIPI clock input |
| 19 | GND | Digital ground |
| 20 | D1P | MIPI data input. |
| 21 | D1N | MIPI data input. |
| 22 | GND | Digital ground |
| 23 | D0P | MIPI data input. |
| 24 | D0N | MIPI data input. |

| | | |
|----|------------|---|
| 25 | GND | Digital ground |
| 26 | STBYB | Standby mode. STBYB = "H", normal operation(default) STBYB = "L", timing controller, source driver will turn off, all output are GND. |
| 27 | RESET | Global reset pin. Active Low to enter Reset State. Normally pull high. Connecting with an RC reset circuit for stability. |
| 28 | VDD (1.8V) | Digital power |
| 29 | VDD (1.8V) | Digital power |
| 30 | VCOMI | Common voltage |

2. PCAP PIN Definition

| Pin | Symbol | Function |
|-----|------------|--------------------------------|
| 1 | USB_VSS | System ground |
| 2 | USB_VDD 5V | Power supply |
| 3 | USB_D+ | Data + |
| 4 | USB_D- | Data - |
| 5 | VSS | System ground |
| 6 | SDA | I2C data input and output |
| 7 | SCL | I2C clock input |
| 8 | RST | External Reset, Low is active |
| 9 | INT | External interrupt to the host |
| 10 | VDDT 3.3 | Power supply |

Note: Interface can support both USB and I2C, USB is main function

Note 2 : Connect VSS(USB_VSS) of CTP with TFT GND

Contour Drawing

